PATENT

N1280-00025
[TSMC2002-1189]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Yi-Lung Cheng et al.**

Examiner: **Richard A. Booth**

Serial No.: **10/716,818**

Group Art Unit: **2812**

Filed: **November 19, 2003**

Confirmation No.: **8692**

For: **METHOD AND SYSTEM FOR FABRICATING A COPPER BARRIER LAYER WITH LOW DIELECTRIC CONSTANT AND LEAKAGE CURRENT**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

DECLARATION OF YING-LANG WANG UNDER 37 CFR 1.131

1. My name is **Ying-Lang Wang**. I am currently an employee of Taiwan Semiconductor Manufacturing Co., Ltd. ("TSMC"), the assignee of the present application.

2. I am a joint inventor with **Yi-Lung Cheng** (collectively, "We") of the subject matter disclosed in U.S. Patent Application Serial No. 10/716,818, filed November 19, 2003, entitled "Method and System for Fabricating a Copper Barrier Layer with Low Dielectric Constant and Leakage Current" (the "Application").

3. I submit this Declaration to the United State Patent Office under 37 C.F.R. 1.131 to swear behind U.S. Published Application No. 2004/0203176A1 to Zhao et al., which has a United States effective filing date of April 9, 2003 and which is relied on by the Examiner in the Official Action dated September 8, 2005 in rejecting pending Claims 1-8, 10-11, 13 and 24-25 as being obvious.

4. All of the events outlined below occurred in Taiwan, R.O.C. and after Taiwan, R.O.C. became a WTO country in January 2002.

5. Before April 9, 2003, we conceived of a new method for reducing metal diffusion in a semiconductor device as described in the Application.

6. Prior to April 9, 2003, we reduced to practice our method of reducing metal diffusion in a semiconductor device comprising forming a copper containing metal portion over a substrate; forming a silicon carbon nitro-oxide (SiCNO) layer on the copper containing metal portion; depositing a first dielectric layer over the SiCNO layer; and generating an opening in the SiCNO layer and the first dielectric layer for a connection metal portion to be connected to the copper containing metal portion, wherein the SiCNO layer reduces the diffusion of the copper containing metal portion into the first dielectric layer.

7. Prior to April 9, 2003, we reduced to practice an embodiment of our method detailed in Paragraph 6 wherein the forming a SiCNO layer step is performed in a PECVD chamber.

8. Prior to April 9, 2003, we reduced to practice an embodiment of our method detailed in Paragraph 6 wherein the forming a SiCNO layer step includes: depositing a Si based precursor layer; and exposing the precursor layer to predetermined gases providing C, N, and O elements to form SiCNO.

9. Prior to April 9, 2003, we reduced to practice an embodiment of our method detailed in Paragraph 8 wherein the predetermined gases include $SiH(CH_3)_3$, CO_2 or O_2, and NH_3.

10. Prior to April 9, 2003, we reduced to practice an embodiment of our method detailed in Paragraph 8 wherein the SiCNO is formed under a pressure between 2 and 4 Torr with a temperature between 325 and 400 °C.

11. Prior to April 9, 2003, we reduced to practice an embodiment of our method detailed in Paragraph 6 wherein the generating step includes: etching the first dielectric layer and the SiCNO layer to form a trench region and a via region; and depositing the connection metal portion into the trench and via regions.

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13. Prior to April 9, 2003, we reduced to practice an embodiment of our method detailed in Paragraph 6 comprising reducing the first dielectric layer to a predetermined thickness; depositing a SiCNO based etch stop layer on top of the reduced first dielectric layer; and depositing a second dielectric layer on top of the etch stop layer.

14. Prior to April 9, 2003, we reduced to practice an embodiment of our method detailed in Paragraph 13 wherein the generating step includes: etching the first and second dielectric layers and the SiCNO based etch stop layer to form a trench region and a via region; and depositing the connection metal portion into the trench and via regions.

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16. Prior to April 9, 2003, we reduced to practice our method for reducing copper diffusion in a semiconductor device comprising: depositing a copper containing metal layer on top of a substrate; depositing a Si based precursor layer on top of the copper based metal layer; exposing the precursor layer to predetermined gases to form a silicon carbon nitro-oxide (SiCNO) layer; depositing a first dielectric layer on top of the SiCNO layer; reducing the first dielectric layer to a predetermined thickness; depositing a SiCNO based etch stop layer on top of the reduced first dielectric layer; depositing a second dielectric layer on top of the etch stop layer; etching the first and second dielectric layers and the SiCNO based etch stop layer to form a trench region and a via region; depositing a predetermined metal into the trench and via regions to contact the copper based metal layer; wherein the SiCNO layer prevents the diffusion of the copper based metal layer into the first dielectric layer.

17. Prior to April 9, 2003, we reduced to practice an embodiment of our method detailed in Paragraph 15 further comprising depositing on top of the trench a sealing SiCNO layer that seals the trench and second dielectric layer thereunder.

18. In January 2003, I understand that TSMC forwarded an invention disclosure record to our patent counsel, Duane Morris LLP, for preparation of the Application. The invention disclosure record included a PowerPoint® presentation dated January 8, 2003 (the "Presentation") documenting our invention and referencing some tests we performed reducing the invention to practice. The Presentation is attached as Exhibit A.

19. Exhibit B contains a labeled version of Slide 6 from the Presentation, which we have updated to label the Cu, SiCNO and low K dielectric layers shown in the SEM (scanning electron microscope) picture shown in Slide 6.

20. The tests we performed referenced in Paragraph 18 embodied our method for reducing copper diffusion in a semiconductor device as detailed in Paragraphs 6-17.

21. As can be seen in, for example, Exhibit A, Page 6 and Exhibit B, we formed a copper containing metal portion (labeled "Cu" in Exhibit B). The copper containing metal portion was formed over a substrate (not shown). We formed a silicon carbon nitro-oxide (SiCNO) layer (labeled "SiCNO" in Exhibit B) on the cooper containing metal portion. We deposited a first dielectric layer (labeled "LK" (for "low-K") in Exhibit B) over the SiCNO layer. We generated an opening as detailed below in the SiCNO layer and the first dielectric layer for a connection metal portion to be connected to the copper containing metal portion as illustrated by the via shown in Exhibit B. At the time, we understood the SiCNO layer to reduce the diffusion of the copper containing metal portion into the first dielectric layer. We utilized a PECVD chamber in forming the SiCNO layer. We deposited a Si based precursor layer and exposed the precursor layer to gases providing C, N, and O elements. In the exposing step, we used a gas mixture of $SiH(CH_3)_3$, CO_2 and NH_3 in one test run. In a second test run, we used a gas mixture of $SiH(CH_3)_3$, O_2 and NH_3. The pressure was set between 2.5 to 3 Torr and test runs were made at 325°C, 350°C and 400°C. Although only an etched via region is shown in Exhibits A and B, we used a dual damascene interconnect formation process for forming both via and trench regions and for filling those regions with a connection metal. We then formed a sealing SiCNO

layer on the top of the deposited connection metal portion and dielectric layer. In one test, as part of the damascene process, we etched the first dielectric layer and SiCNO layer to form a trench and a via region. In a second test, as part of the damascene process, we reduced the first dielectric layer to a predetermined thickness, deposited a SiCNO based etch stop layer on top of the reduced first dielectric layer, and deposited a second dielectric layer on top of the etch stop layer. The opening was generated by etching the first and second dielectric layers and the SiCNO based etch stop layer to form a trench region and a via region. We then deposited the connection metal portion into the trench and via regions and deposited on top of the connection metal portion a sealing SiCNO layer that seals the connection metal portion and the second dielectric layer thereunder.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18, United States Code, Section 1001, and that such willful false statements may jeopardize the validity of the above-identified application or any patent issuing thereon.

DATE: _____ Ying-Lang Wang

Ying-Lang Wang

02-1189

A Novel Cu Barrier Layer with lower Dielectric Constant and Leakage Current

TFE 鄭義榮
TFE 王英郎

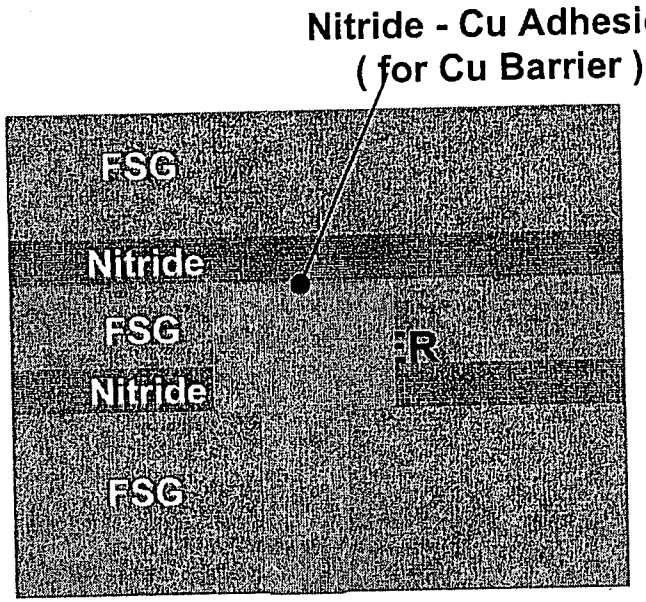
New Cu Barrier layer Development (SiCNO) Executive Summary

- **New Cu Barrier layer Development (SiCNO) has developed:**
  - Doping Oxygen/Carbon/Nitrogen into Si source.
  - High density film.
  - Decrease Dielectric constant.
  - Lower leakage current.
  - Well integration with Cu process.

New Cu Barrier layer Development (SiCNO)

■ Background:

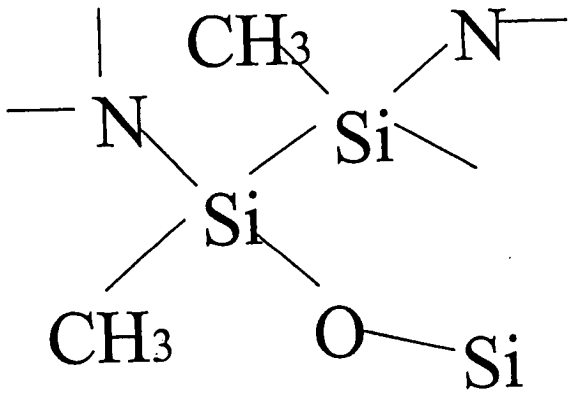
- In Cu process, it needs Cu barrier and etch stop layer to prevent Cu diffusing.
- Silicon nitride was commonly used, the advantage is K=7.0 , which the merit of Cu interconnect has been degraded by the parasitic capacitance effect.



New Cu Barrier layer Development (SiCNO)

■ Patent Claim:

1. Doping Oxygen/Carbon/ Nitride on Si precusor
2. Decrease the dielectric constant, lower than Silicon-Nitride (SiN) / Silicon Carbide (SiC)



Dielectric constant Comparison for diffent Cu barrier layer

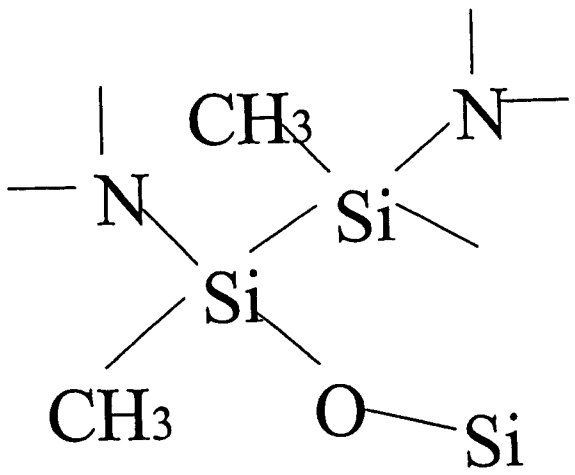
Film Type	K value
SiN	7.2
SiC	4.82
* SiCNO	4.27

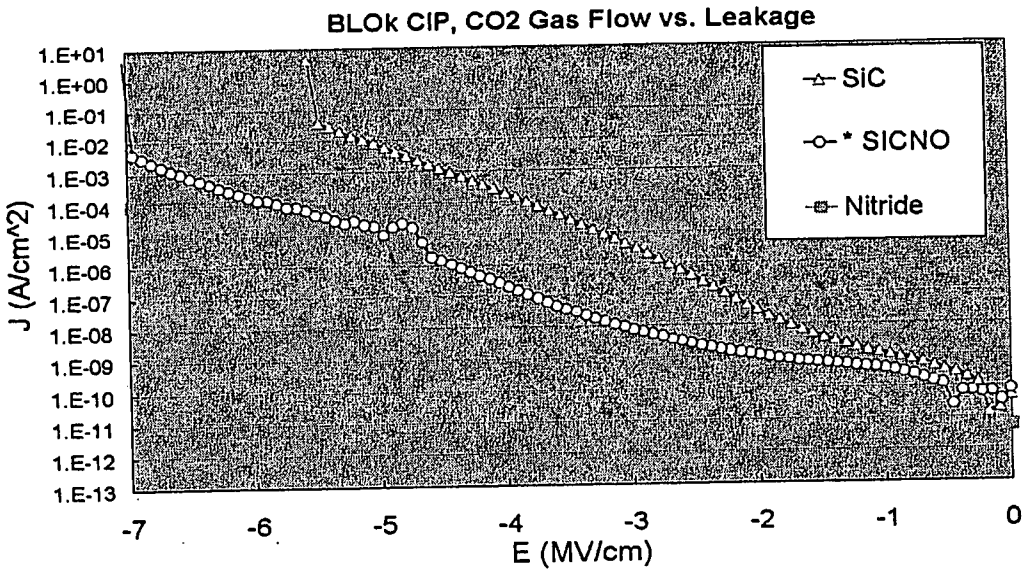
* Measured by Hg Probe

New Cu Barrier layer Development (SiCNO)

■ Patent Claim:

- Due to Si-O net work, lower the leakage current.
- Lower Break-down voltage (J=1E-4) : SiC : 3.8V, SICNO:5.9V, SiN=7V
- SiCNO is suitable for LK process



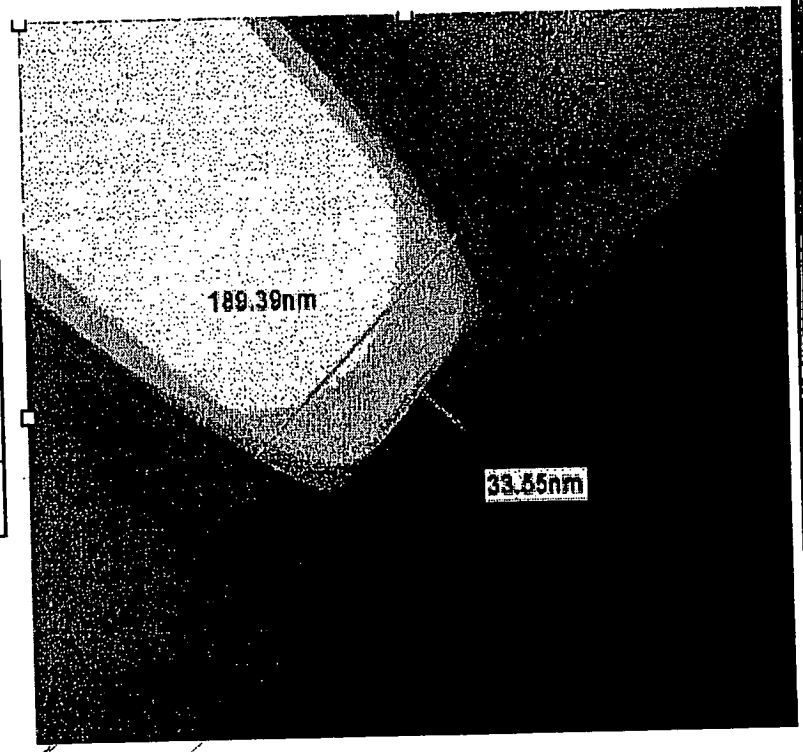


New Cu Barrier layer Development (SiCNO)

■ Patent Claim:

- **High Film Density. High via etch selectivity.**

Condition	Density	Via Dry Etch Rate(30S)	Via Dry Etch Rate(A/min	Selectivity
BD		1354	2708	
SiC	1.7807	246	492	5.23171
* SiCNO	1.825	206	412	6.24757



New Cu Barrier layer Development (SiCNO)

■ Patent Claim:

- **Better Film Stability : High resistance against Heat/Moisture.**

	Test	RI	K	RI	K	RI	K
SiCNO	Alloy 400C, 7times	1.7721	4.28	1.7724	4.28	0.0003	0
SiCNO	PCT (120C ,100%RH,168hr)	1.7734	4.26	1.7822	4.38	0.0088	0.12
SiCNO	Ashing(O2/CO2)	1.7728	4.26	1.7732	4.27	0.0004	0.01

New Cu Barrier layer Development (SiCNO)

■ Patent Claim:

- **Adhesion between Cu : Better than SiC, comparable with SiN**
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Sample	Substrate	DNS	Barrier	Meas.A	Meas.B	Meas.C	Avg(Kg/cm2	Ave(Mpa)
1	Thox THK							
2	Cu	V	SiN	782	738	736	752	73.7
3	Cu	V	SiC	249	401	353	334	32.8
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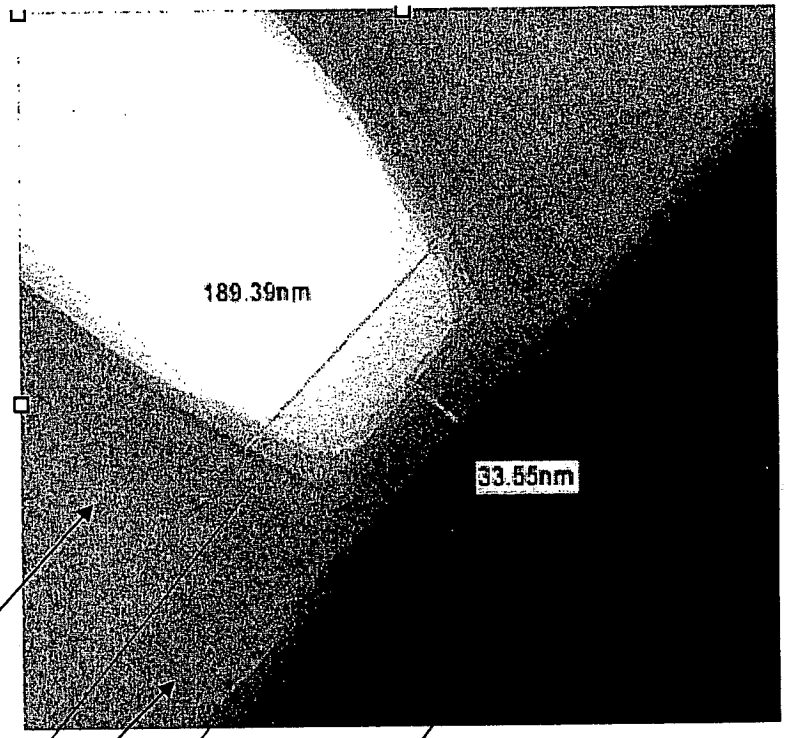

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DATE: 2006/1/04

Yi-Lung Cheng

Yi-Lung Cheng

Exhibit A: PowerPoint® presentation dated January 8, 2003

Exhibit B: Labeled version of Slide 6 of Exhibit A dated December 13, 2005.

02-1189

A Novel Cu Barrier Layer with lower Dielectric Constant and Leakage Current

TFE 鄭義榮
TFE 王英郎

New Cu Barrier layer Development (SiCNO) Executive Summary

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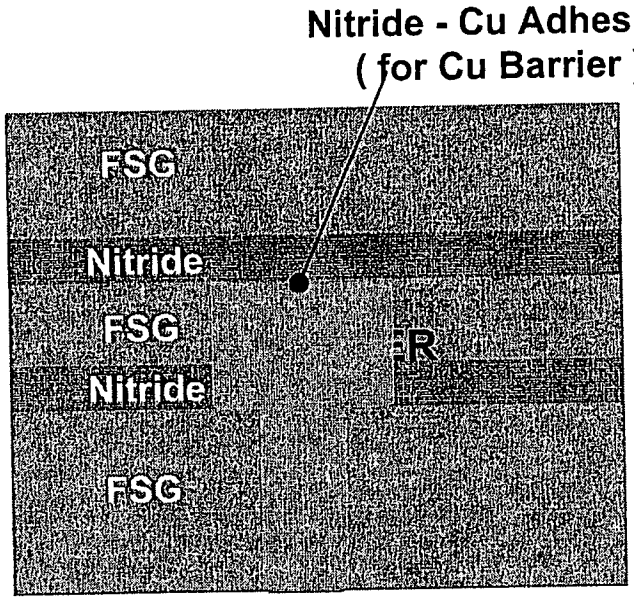

New Cu Barrier layer Development (SiCNO)

■ Patent Claim:

1. Doping Oxygen/Carbon/ Nitride on Si precusor
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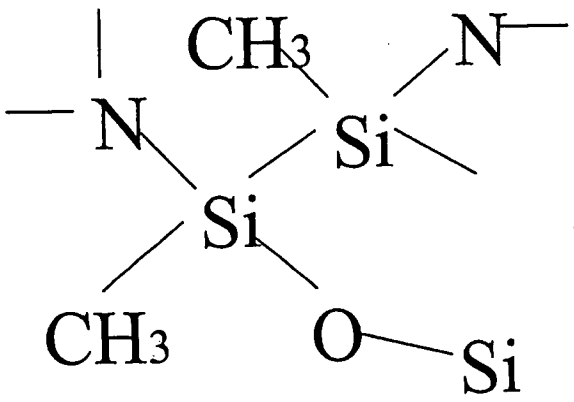

Dielectric constant Comparison for diffent Cu barrier layer

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- Due to Si-O net work, lower the leakage current.
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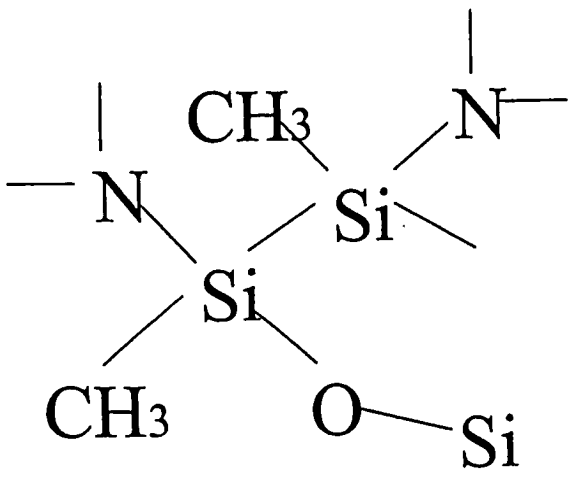
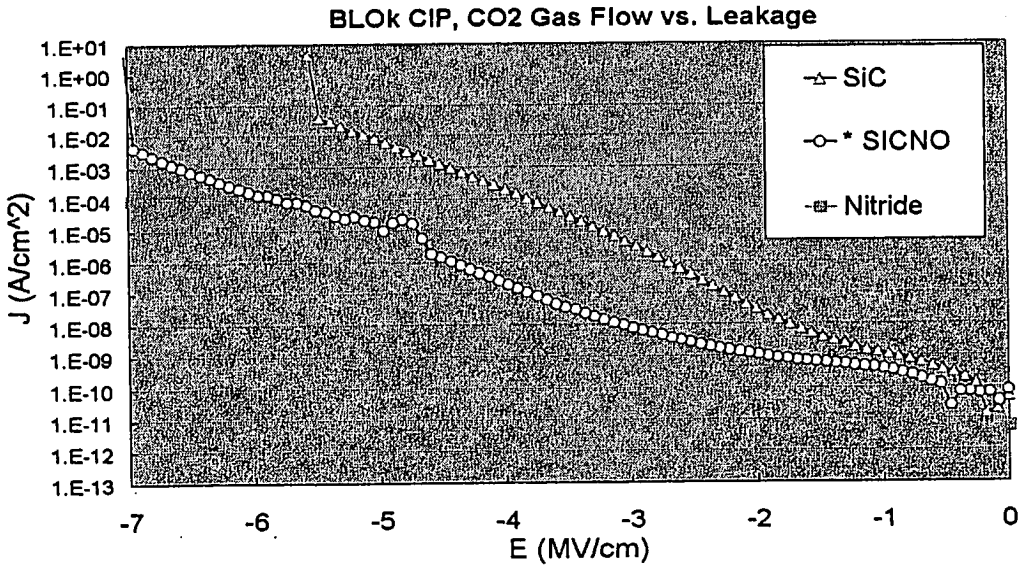
- SiCNO is suitable for LK process





New Cu Barrier layer Development (SiCNO)

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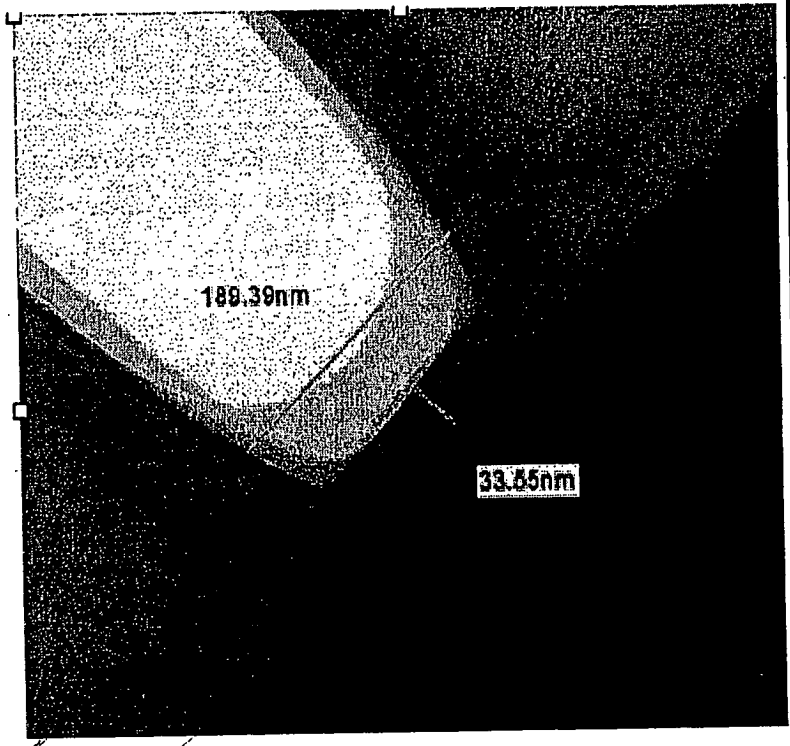

New Cu Barrier layer Development (SiCNO)

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- **Better Film Stability : High resistance against Heat/Moisture.**

	Test	RI	K	RI	K	RI	K
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SiCNO	PCT (120C ,100%RH,168hr)	1.7734	4.26	1.7822	4.38	0.0088	0.12
SiCNO	Ashing(O2/CO2)	1.7728	4.26	1.7732	4.27	0.0004	0.01

New Cu Barrier layer Development (SiCNO)

■ Patent Claim:

- **Adhesion between Cu : Better than SiC, comparable with SiN**
-

Sample	Substrate	DNS	Barrier	Meas.A	Meas.B	Meas.C	Avg(Kg/cm2	Ave(Mpa)
1	Thox THK							
2	Cu	V	SiN	782	738	736	752	73.7
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